APATCO Technologies

NCS EB50

- **Single Board 8 or 16 bit Computer**
- **W65C02S and W65C816S compatible**
- **Compatible with WDC ViaUSB device**

Introduction

The NCS-EB50 is a printed circuit board designed to accept many of the components from the NCS-2056T breadboard computer kit. It allows for **permanent mounting** of these components on a PCB.

NCS-EB50 expands on capabilities of the NCS-2056T by adding a second I/O chip in the form of a W65C22N VIA. This chip allows for a **GPIO port**, compatible with Western Design Center products, including the **ViaUSB adaptor.**

A larger EEPROM is also part of the NCS-EB50. Instead of the 8KB EEPROM used in the NCS-2056T, the NCS-EB50 is designed for a **32KB** EEPROM.

Additional connectors include 8 pin **Serial I/O port**, a 6 pin **I/O control port**, and a 50 pin **memory bus expansion connector**. A 20 pin LCD connector and PS/2 connector are also included.

The CPU socket (U1) is designed to accept both the 8-bit W65C02S as well as the 16-bit **W65C816S**. The W65C816S memory can be de-multiplexed using the 50 pin memory expansion bus.

NCS 2056T Re-usable Components

W65C02S CPU, W65C22N VIA, CY7C199CN RAM, AT28C64B EEPROM, 7404 Hex-Inverter, 74LS00 NAND, 74LS138 De-coder, Reset IC, Voltage Regulator, 1K resistors, 3K resistors, LED, AGM2864F LCD Module.

Features

- Dual Oscillators (use gate circuit from NCS 2056T, or use canned oscillator)

- 8 or 16 bit processor (W65C02S & W65C816S) up to 20Mhz

- 64KB memory on board (32KB RAM & 32KB ROM)

- 16MB memory possible when using W65C816S and 50 pin memory connector

- Dual W65C22S VIAs providing (LCD connector, PS/2 port, Serial connector, GPIO connector)

- 256 bytes from top of RAM decoded to 8 lines (accessible via J4 & J6 connector)

- 50 pin memory bus connector for future options like VGA and Memory Expansion

Memory Map

Hex Address Decimal	Bytes	Chip	74LS138
0000h - 7EFFh (0 - 32511)	32512 bytes	32KB RAM	
7F00h - 7F0Fh (32512 – 32543)	32 bytes	VIA1 (U3) (only 16 bytes)	/Y0
7F20h – 7F2Fh (32544 – 32559)	32 bytes	VIA2 (U2) (only 16 bytes)	/Y1
7F40h – 7FFFh (32576 - 32767)	192 bytes	not used but mapped	/Y2 - /Y7
8000h - FFFFh (32768 – 65535)	32768 bytes	32KB EEPROM	

LCD Connector (J1)

1	Vss
2	Vdd (+5V)
3	To Pin 1 of 20K pot
4	PB3 (U3)
5	3K Pull-Down
6	PB0 (U3)
7	PA0 (U3)
8	PA1 (U3)
9	PA2 (U3)
10	PA3 (U3)
11	PA4 (U3)
12	PA5 (U3)
13	PA6 (U3)
14	PA7 (U3)
15	PB1 (U3)
16	PB2 (U3)
17	RESB
18	To Pin 2 of 20K pot
19	Ground
20	PB6 (U3)

Power (J2)

1	+5V
2	Ground

GPIO Connector (J3)

1	Vdd (+5V)
2	Vdd (+5V)
3	Vss
4	Vss
5	CA1 (U2)
6	CA2 (U2)
7	PA0 (U2)
8	PA1 (U2)
9	PA2 (U2)
10	PA3 (U2)
11	PA4 (U2)
12	PA5 (U2)
13	PA6 (U2)
14	PA7 (U2)
15	CB1 (U2)
16	CB2 (U2)
17	PB0 (U2)
18	PB1 (U2)
19	PB2 (U2)
20	PB3 (U3)
21	PB4 (U3)
22	PB5 (U3)
23	PB6 (U3)
24	PB7 (U3)
25	Vss
26	Vss
27	Vdd (+5V)
28	Vdd (+5V)

Memory Bus Connector (J4)

1	Vss	26	RWB
2	Vss	27	U7 E3
3	Vdd (+5V)	28	PHI2O / VDA
4	Vdd (+5V)	29	D0
5	A0	30	D1
6	A1	31	D2
7	A2	32	D3
8	A3	33	D4
9	A4	34	D5
10	A5	35	D6
11	A6	36	D7
12	A7	37	PHI10 / ABORTB
13	A8	38	VPA
14	A9	39	RESB
15	A10	40	BE
16	A11	41	RDY
17	A12	42	MLB
18	A13	43	IRQB
19	A14	44	NMIB
20	A15	45	SYNC / VP
21	U5 CE	46	PHI2
22	U4 CE	47	Vdd (+5V)
23	U3 CS	48	Vdd (+5V)
24	U2 CS	49	Vss
25	U7 /Y2	50	Vss

Serial Connector (J5)

1	Vss
2	Vdd (+5V)
3	Vss
4	CA1 (U3)
5	CA2 (U3)
6	CB1 (U3)
7	CB2 (U3)
8	PB7 (U3)

I/O Control Port (J6)

1	Vss
2	/Y3 (U7)
3	/Y4 (U7)
4	/Y5 (U7)
5	/Y6 (U7)
6	/Y7 (U7)

PS/2 Port (CN1)

1	Data (PB5)
2	NC
3	GND
4	+5V
5	Clock (PB4)
6	NC

JP1	JP2	JP3	JP4	JP5	JP6	R15	SW1	TP1
Enable or Disable ROM Disable routes CE to pin 2 of control connector.	Enable or Disable RAM Disable routes CE to pin 3 of control connector.	Selects Chip Select for U2 (VIA2) to U7 or J4	Selects Internal Enable for U7 or External EnableJ4	Selects Chip Select for U3 (VIA1) to U7 or J4	Selects between Oscillator Circuits	LCD Contrast	Reset Switch	Test point, connected to NMI

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